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A Comparative Study of TEGFET and MESFET Large Signal Characteristics and Saturation Mechanisms

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ABSTRACT

A new method for large-signal transistor analysis is presented and applied to TEGFETs and MESFETs. Saturation mechanisms of both types of transistors are described and operation differences are discussed. The importance and influence of higher harmonic signal components on the large signal characteristics is also shown.

INTRODUCTION

GaAs MESFETs have for long been the traditional three-terminal devices for microwave power applications. Another potential candidate, initially recognized for its excellent low-noise characteristics only, is the Two - Dimensional - Electron - Gas FET (TEGFET). GaAs/AlGaAs multiple heterojunction TEGFETs have demonstrated very good characteristics for power applications, especially at high frequencies. Saunier (1) has reported at 32.5 GHz a power of 0.6 W/mm, a gain of 5.4dB and a power - added efficiency of 30%. The same device at 60 GHz had a power of 0.4 W/mm, a gain of 3.6 dB and a power - added efficiency of 14%. TEGFETs are also very well suited for integrated circuit applications (2), (3). It is therefore important to study their large-signal characteristics and saturation mechanisms in order to understand better their operation and achieve optimum power performance. Furthermore, a simultaneous examination of similar effects in MESFETs allows a better understanding of the relative merits of each technology. These aspects have been examined both theoretically and experimentally and are presented in this paper.

POWER PREDICTION FROM SMALL-SIGNAL MEASUREMENTS

To investigate the large-signal properties of FETs, the S-parameters of devices realized in our laboratories were measured in the 2-18 GHz range for various gate-source and drain-source bias conditions V_{gs} and V_{ds}.
The transistors were multi-finger structures with 0.5 um gate length and 75 um finger width for the TEGFETS and 1 um gatelength and 150 um fingerwidth for the MESFET.
Interpolation functions fitting the voltage dependent characteristics of equivalent circuit parameters were then determined. The technique applied to g_m, G_{ds}, C_{gs} and C_{dg}. Gate forward conduction and gate-drain breakdown were simulated by conductances G_{gf}, G_{dg} connected in parallel to C_{gs} and C_{dg} (4). The power dependent "large-signal" parameters were evaluated as average instantaneous values over a signal period as reported in (5), (6). They have been obtained by taking into account the first and second harmonic of the basic frequency. Fig. 1 shows the measured and calculated power characteristics of a MESFET at the basic and higher harmonic frequencies. Calculations neglecting higher harmonics underestimate the saturation power. The agreement can be impoved by taking into account two or more harmonics. Their dependence on the input power level agrees qualitatively with the results reported by Willing (7). Similar results were also obtained for TEGFETs.Fig. 2 shows measured and calculated Load-Pull contours of the same MESFET. The latter were obtained without taking into consideration higher harmonics. The gain corresponding to the load contours is 0.75dB smaller than the optimum.

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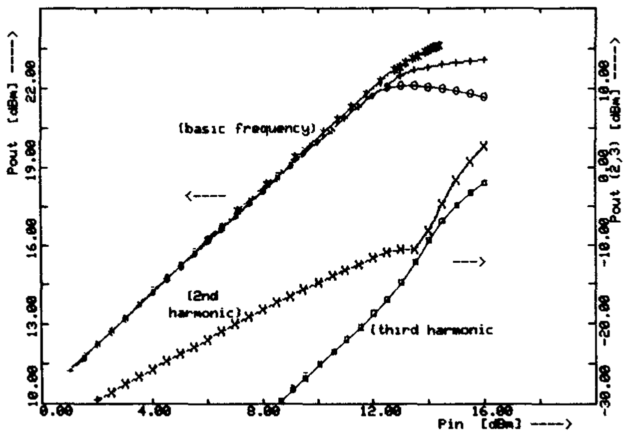

Fig.1: Measured (*) and calculated output versus input power characteristics of MESFET (:3rd, x:2nd, O:1st (basic) harmonic power, +: calculation with all three harmonics for f=6GHz)

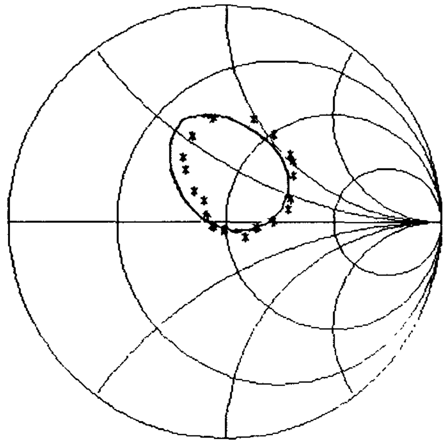

Fig 2 Load-pull contours of MESFET measurement, -.theory), f=6GHz, Vds=7 , Vgs=-0 83V

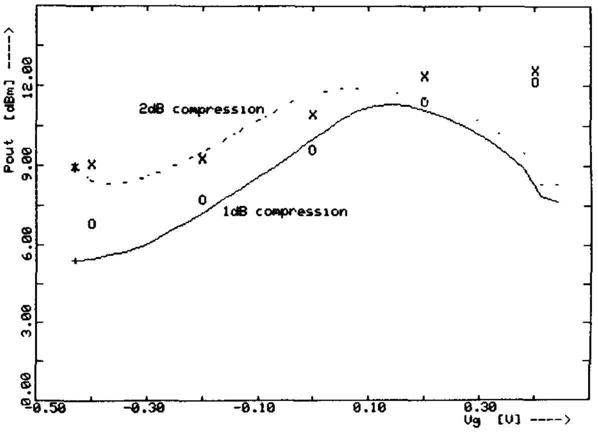

Fig.3: TEGFET saturated output power as a function of gate bias Vgs, f=8GHz, Vds=5V, Zin=Zout=50ohms

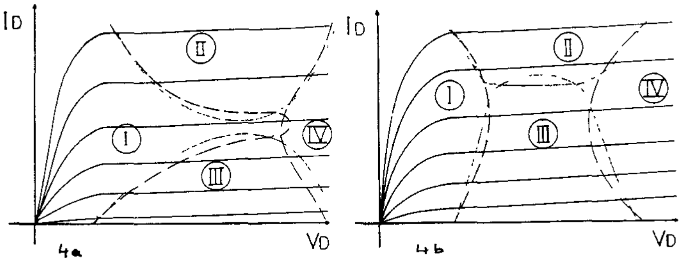

Fig.4: MESFET (a) and TEGFET (b) operating regions according to saturation mechanism by (I):Gds, (II):Ggf, (III):gm, (IV):Gdg

The agreement between calculations and measurements is excellent, suggesting that the inclusion of higher harmonics is primarily important for the prediction of saturation characteristics but not necessarily for load contours.

Fig. 3 shows gate-bias dependence of TEGFET output power at 1dB and 2dB gain compression. To achieve a better measurement reproducibility and eliminate inaccuracies due to not exactly known loads, TEGFETs were terminated by 50 ohms at both input and output. Good agreement between simulation and measurement can be observed up to gate voltages V_{gs}=0.2V. For higher gate-bias, the theoretically predicted output powers are lower than the experimental due to the overestimation of forward current by the continuosly assumed exponential diode characteristics.

SATURATION MECHANISMS

Our simulations show that there are basically four different mechanisms which may cause power saturation of transistors. These can be classified according to bias conditions and are illustrated for TEGFETs and MESFETs in regions (I) to (IV) of Fig. 4:

Region (I): Here the the V_{ds}-bias is relatively small and lies close to the linear region of the I_{ds}-V_{ds}-characteristics. Any large output-voltage swings occuring under large signal conditions will very easily lead to partial operation in the linear region of the I_{ds}-V_{ds} curves. This is responsible for limiting the output power and causes FET saturation. In terms of device parameter characteristics, this operation

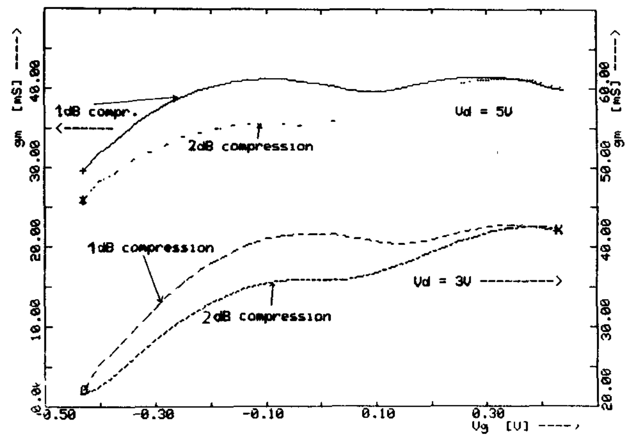

Fig.5: TEGFET transconductance gm at satruation as a function of gate bias Vgs, f=8GHz, Vds=5V, Zin=Zout=50ohms

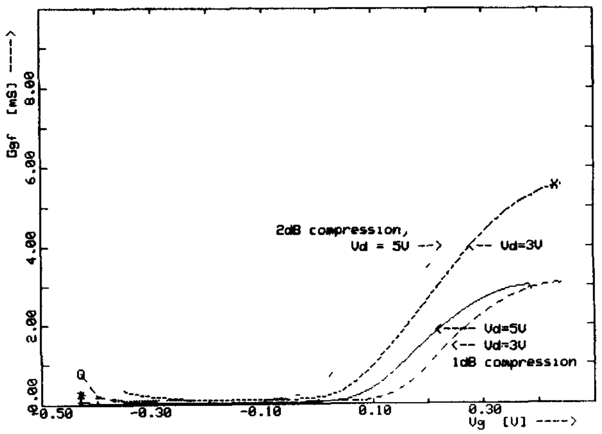

Fig 6 TEGFET diode forward conductance Ggf at saturation as a function of gate bias Vgs, f=8GHz, Vds=3.5V, Zin=Zout=50ohms

is indicated by large power-dependent G_{ds}-values.

Region (II): Here, a near-zero or even positive gate-bias V_{gs} is chosen in order to obtain large I_{ds} currents. A large input power swing will cause partial forward operation of the gate-source diode and will induce output power saturation. This effect is associated to large values of gate-source forward conductance.

Region (III): A large negative V_{gs} bias is employed in this near to pinch-off region. Large input-powers will cause even closer operation to pinch-off. Since g_m is here very small, the transistor cannot provide high gains. The output power saturates due to large-signal g_m-values decreasing with input level.

Region (IV): The drain-source bias V_{ds} is here relatively large and close to the breakdown voltage. Large output-voltage swings will be limited by gate-drain avalanche and will lead to saturation of the output power. This saturation mechanism is associated to gate-drain backward conductance increase.

In practice, all four saturation mechanisms described above are normally present, but generally only one of the mechanisms is predominant, depending on bias condition. In the following we will describe the TEGFET and MESFET large signal features using Figs. 4a and 4b: Region (I) is very large for MESFETs, extending to high Vds values and including Idss/2 operation. For Vgs larger then the corresponding Idss/2 gate voltage, saturation is dominated by partial forward operation of the gate-source diode (region (II)).

TEGFETs have much smaller regions (I) and (II) because of two reasons: (1): Gm compression for near zero or even positive Vgs (caused by partial modulation of electrons in the low-mobility AlGaAs of TEGFETs) results in a gm decrease at high powers.This is much more important in TEGFETs than MESFETs and starts earlier than the Gds increase. Therefore, the TEGFETs region (III) is very large, confining regions (I) and (II) in smaller areas. (2): The TEGFET Schottky-barrier voltage is approximately 0.25V larger than in MESFETs (for an Al-mole fraction x=0.22 of our devices). Slightly higher input voltage swings can therefore be tolerated without causing partial forward operation of the gate-source diode in the TEGFETs and result in a smaller region (II).

Region (IV) of TEGFETs is finally larger than for MESFETs because the TEGFETs avalanche breakdown voltage is usually smaller due to the high doped AlGaAs region.

Figs. 5 and 6 show TEGFET gm and Ggf as function of Vgs bias for two different gain compressions and drain bias Vds. These figures illustrate also quantitatively the results of Fig. 4b. Up to Vgs=0.2V, the large-signal gm at 2 dB gain compression is smaller than the large-signal gm at 1dB compression (gm2<gm1), indicating a large dependence of gm on input power and therefore operation in region (III) For larger Vgs, the difference between gm1 and gm2 decreases. The gate-source diode is now responsible for saturation. This can be seen in Fig. 6 by the large power dependent Ggf-values and corresponds to operation in region (II). The similarity of gm vs. Vgs characteristics for two different drain voltages suggests that the predominant saturation mechanisms are due to gm and Ggf rather than Gds and Gdg.

If the operating bias is chosen for maximum gain, then both TEGFETs and MESFETs show power saturation due to G_{gf}

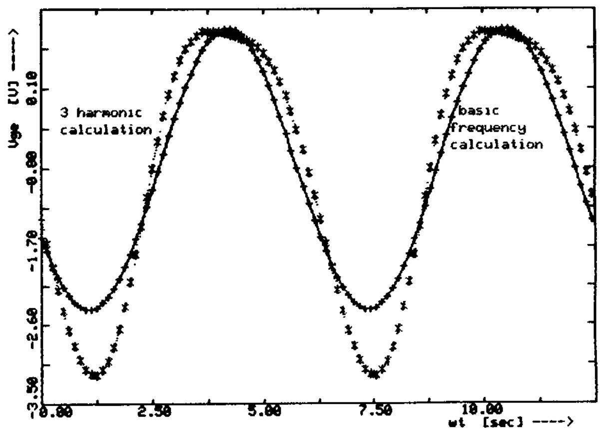

Fig.7: External gate-source voltage Vgs of MESFET at basic frequency (+) and with consideration of three harmonics (*)

(region (II) of Fig. 4). With bias conditions suitable for maximum output power, this saturation is seen to occur due to either Ggf, Gds for MESFETs (regions (II) and (I)) or Ggf, gm for TEGFETs (regions (II) and (III)).

The saturated power characteristics depend on the bias conditions and vary at different rates according to the device type. The output power increases initially almost linearly with Vds and then tends to saturate. This is reported to occur in MESFETs because of performance degradation by channel heating (8). This effect is smaller in TEGFETs especially at lower frequencies. For both devices output power saturation occurs at smaller input levels with increasing frequency.

The output power of TEGFETs reaches its maximum for drain voltages relatively close to the knee voltage, especially at very high frequencies. This is, however, not the case in MESFETs, where larger Vds-values are necessary to obtain optimum output power. The power added efficiency and gain of TEGFETs can therefore be better optimized as already demonstrated experimentally (1).

INFLUENCE OF HARMONIC SIGNAL COMPONENTS

Fig. 7 shows time-domain characteristics of the extrinsic gate-source voltage Vge of a MESFET, calculated by neglecting higher harmonics (+), and by taking account the first and second harmonic components (*). The inclusion of the latter results in flattened peak characteristics for positive voltages, indicating that the partial forward operation of the gate-source diode generates harmonic signal components. Moreover, when higher harmonics are neglected, the negative peak-values of Vge are found to be smaller. The amplitude corresponding to the flattened positive cycle is smaller than the basic frequency amplitude. The resulting gate-source diode current Igs determined using exponential-law diode characteristics is therefore smaller than what one could expect by considering the basic frequency only. Similarly, the gate diode forward conductance Ggf has a smaller value when higher harmonics are considered. This results in output power saturation at larger input levels. The Ggf full-harmonic characteristics are in fact responsible for the better experimental and theoretical agreement in the results of Fig. 1.

CONCLUSION

A large-signal analysis has been presented and applied to TEGFETs and MESFETs. By comparing the obtainded results to experimental power saturation characteristics and load-pull contours, good agreement was demonstrated between theory and experiment. The saturation mechanisms of MESFETs and TEGFETs have been analysed: While MESFET saturation is predominantly due to Gds and Ggf increase with the input power, TEGFETs saturate primarily because of gm decrease. Based on our results, the superior power added efficiency of TEGFETs can be explained.

Second and third harmonics have been included in the large-signal analysis. The neglection of higher harmonics was shown to lead to wrong predictions of saturated output power. This is associated to an overestimation of the gate-source current.

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